A Direct Digital Synthesis VFO for HF Bands

The Project in few words

This article presents a VFO wich uses an AD7008 DDS from Analog Device, the device is controlled by an ST62T25 microprocessor from Thomson.

It is suited to work in single conversion rigs equipped with with a 9 MHz IF channel, and I tink it may be considered an "up to date" device, capable to bear comparison with other synthesizers currently used in the best commercial HAM transceivers.

The tuning requires at least a frequency meter and an RF probe.

How it is made

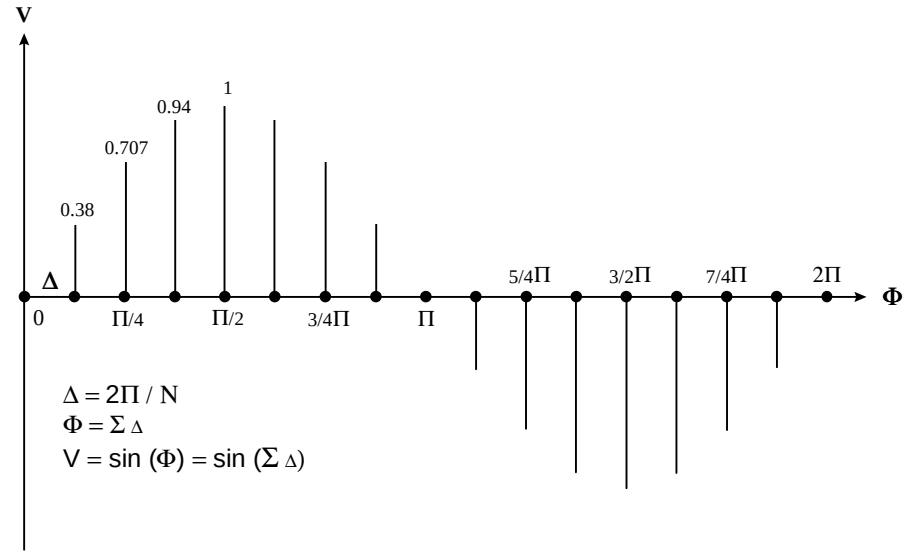
The VFO is composed by three single sided PCB boards 100x70 mm. The two DDS and PLL PCB are stacked into a little aluminium box, while the VCO unit is housed in a separate tin-plate box.
To connect the supply and the digital lines I employed some 2.5 mm spaced linear (comb) connectors, while the signal sources (RF and control voltage to VCO) make use of common RCA sockets.

How it works

The DDS synthesizer is used as a frequency reference for a conventional PLL circuit. This one is implemented with a CMOS 4046 IC wich compares the VCO frequency divided by 64 to the reference frequency coming from the DDS, so controlling the VCO itself. The frequency change required from the DDS spans from 168750 to 609375 Hz, and the corresponding VCO range goes from 10.8 to 39 Mhz.

The DDS frequency synthesis

Now we'll try to understand in a very simple way how the DDS (Direct Digital Sinthesys) works.
Let's suppose we want to draw on a paper sheet all the points of a sinusoidal curve. We'll start dividing the sinusoid period (2Π) in N equal parts. Every segment so obtained (Δ) corresponds to a phase increment equal to 2Π / N and we may calculate the corresponding amplitude value applying the well known formula : V=sin Φ , where Φ = Σ of the Δ segments.

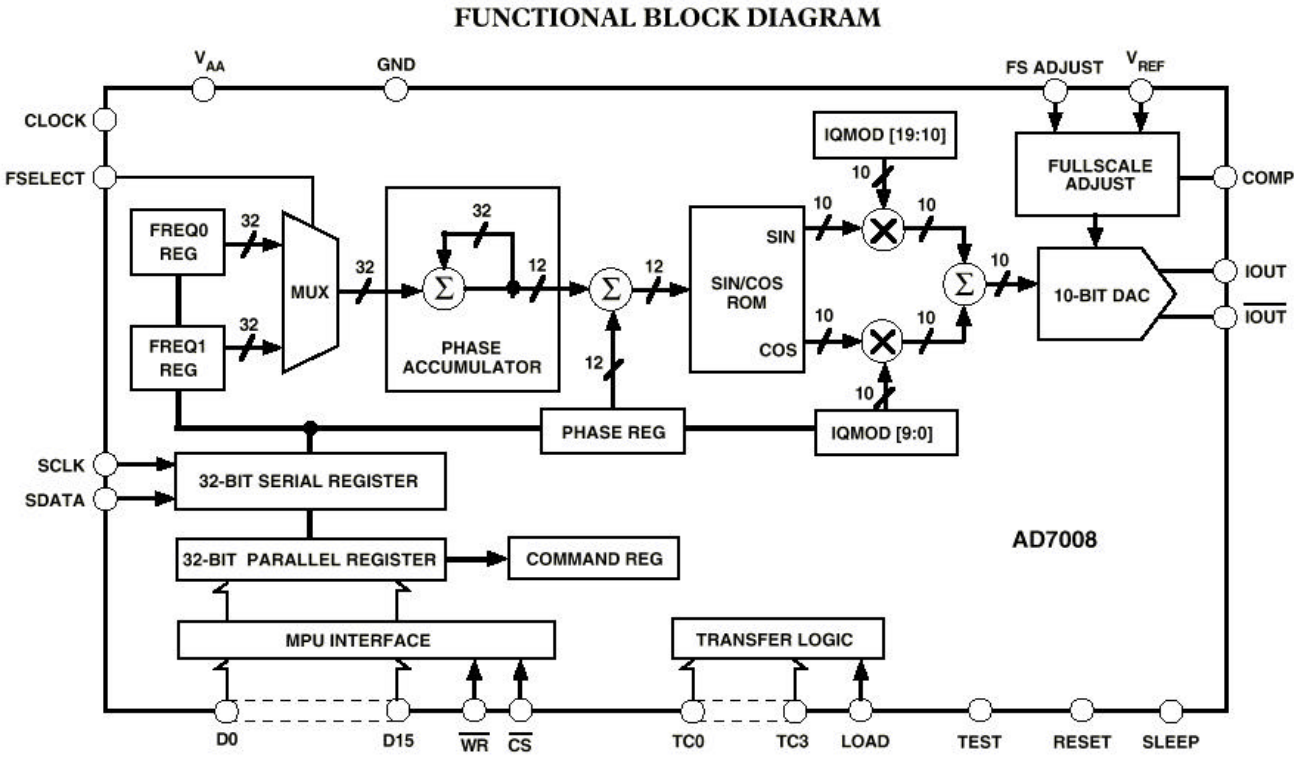


The DDS synthesizer is a special microprocessor wich implements this type of computation. The phase increment Δ is setted by an external control microprocessor through a serial input, and it is stored in a special register called *Phase Accumulator* . This register is increased at every clock cycle by a phase increment Δ. Since this register can hold a 32 bit word, the phase value is expressed as an integer in the range 0 - 2^{32} (corresponding to the interval 0 – 2Π). The corresponding amplitude value is obtained from a ROM resident look-up table, so increasing the calculation speed. At last a DAC converter transform this numerical value into an analog signal.
Now we may draw the relation between the phase increment Δ (a numerical value in the range 0 - 2^{32}) and the DDS generated frequency. The sinusoid period and frequency will be in fact :

$$T = T_{clock} \times (2^{32} / \Delta) \rightarrow F = (\Delta \times F_{clock}) / 2^{32}$$

It is interesting to notice that, using a clock frequency of 50 MHz, the greatest resolution we may obtain with a unitary phase increment Δ will be 50 MHz / 2^{32} = 0.01 Hz.

The AD7008 DDS has also some other functions :
- it may store two frequency values, and switch from one to the other using the FSELECT pin, so we may implement easily the SPLIT function.
- it may generate several modulation types (frequency, amplitude and SSB using the phase shift method) controlling the instant value of the phase and amplitude through some special registers (PHASE REG, IQMOD). To impement theese functions however the modulating signal must be treated first numerically using DSP techniques.



Those who are interested in examining closely this matter may find other informations in the device Data Sheet (see the bibliography at the end).

The Control Software

An ST62T25 microprocessor with a specific software is used to control the DDS, and actually the following functions are avaliable :

- The frequency is controlled by an optical encoder. The default frequency at power-on is setted to 14 Mhz.
- The tuning step may be selected between 3 possible values (10 Hz, 1 Khz and 100 Khz) using two push buttons. The default step is setted to 1 KHz so allowing a fast tuning inside one band, the 10 Hz step is commonly used allowing a 2.5 KHz / turn tuning speed. The 100 KHz step may be used to switch quickly from a band to the other
- The frequency and step values are showed on a 2x16 LCD display
- The band is coded on a 4 bit word and this code is available on 4 microprocessor pins. So you may control an external device like band filters, operational mode, etc..
  The band coding is shown below

	Bit3	Bit2	Bit1	Bit0
Under 3 Mhz	0	0	0	0
From 3 to 6 Mhz	0	0	0	1
From 6 to 9 Mhz	0	0	1	0
From 9 to 12 Mhz	0	0	1	1
From 12 to 17 Mhz	0	1	0	0
From 17 to 20 Mhz	0	1	0	1
From 20 to 23 Mhz	0	1	1	0
From 23 to 27 Mhz	0	1	1	1
From 27 to 29 Mhz	1	0	0	0
Over 29 Mhz	1	0	0	1

In a future software release I expect to implement the following functions :

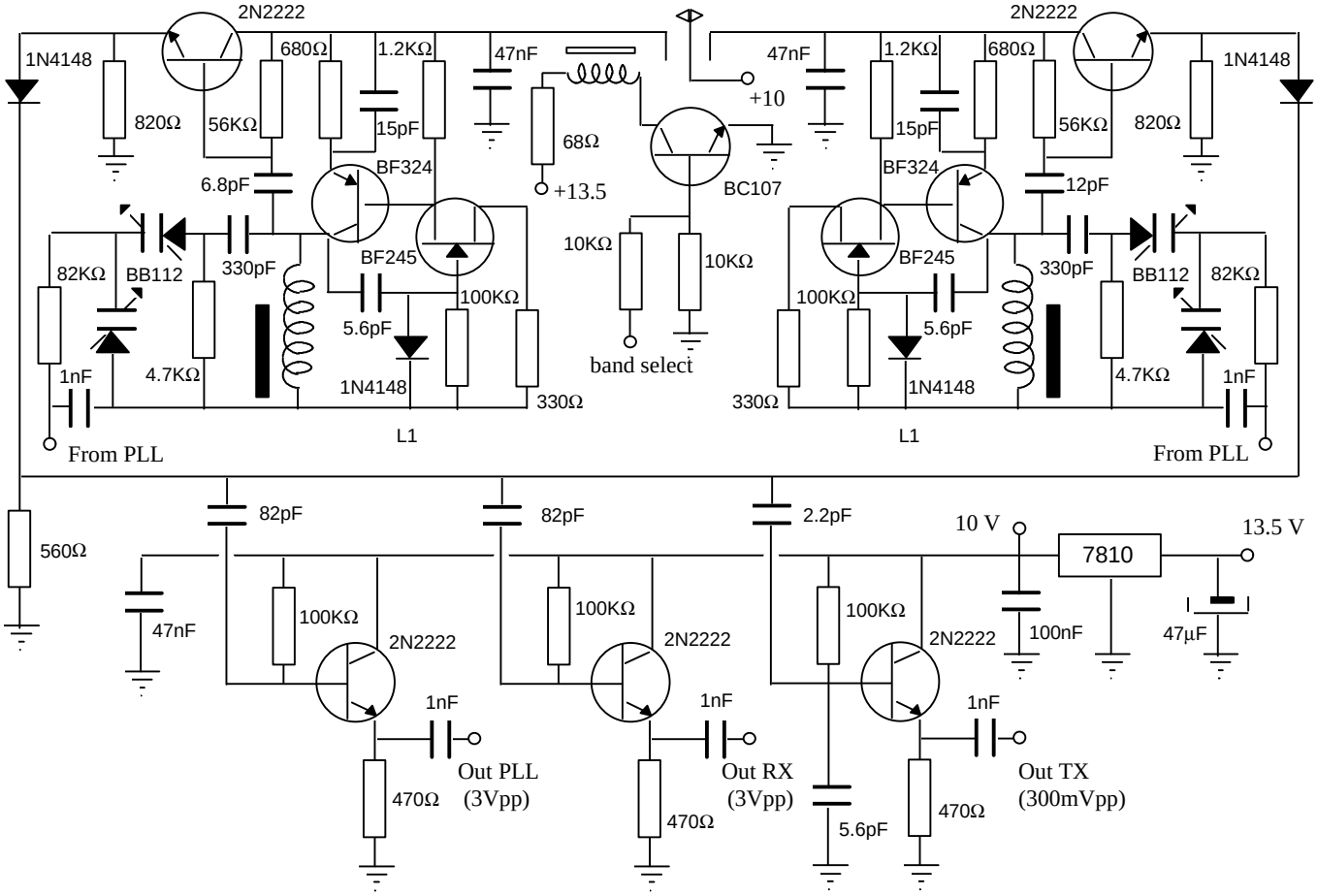
- RIT and XIT operating modes
- Storing and retrieving several operating frequencies by an external serial memory device (ST93C66)

The electrical circuit is already arranged to support theese functions, only the microprocesor will need to be reprogrammed or replaced. The actual software release is available from me via E-mail.

NB. The device is designed for a 9 MHz IF frequency, other values may be used but some simple software changes are required.

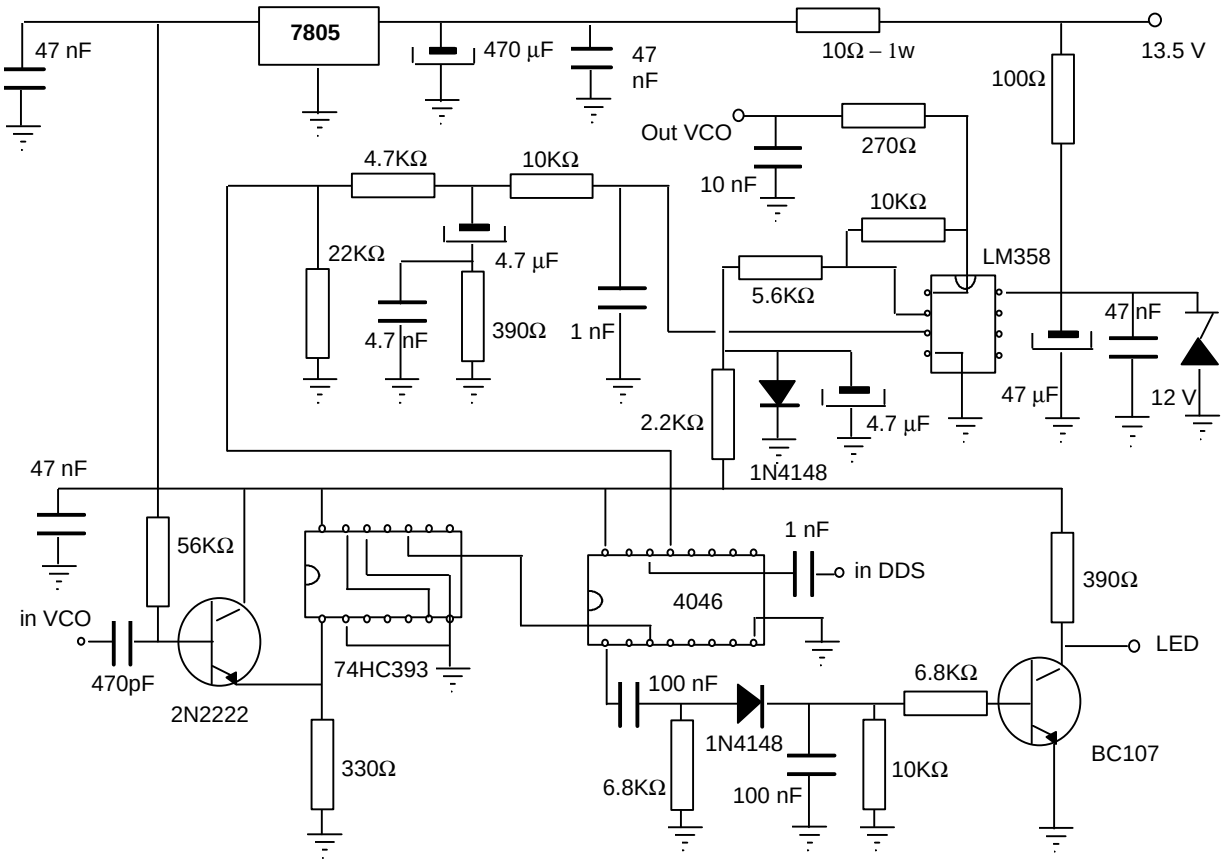
The VCO Module

Now I'll describe the single VFO modules starting with the VCO



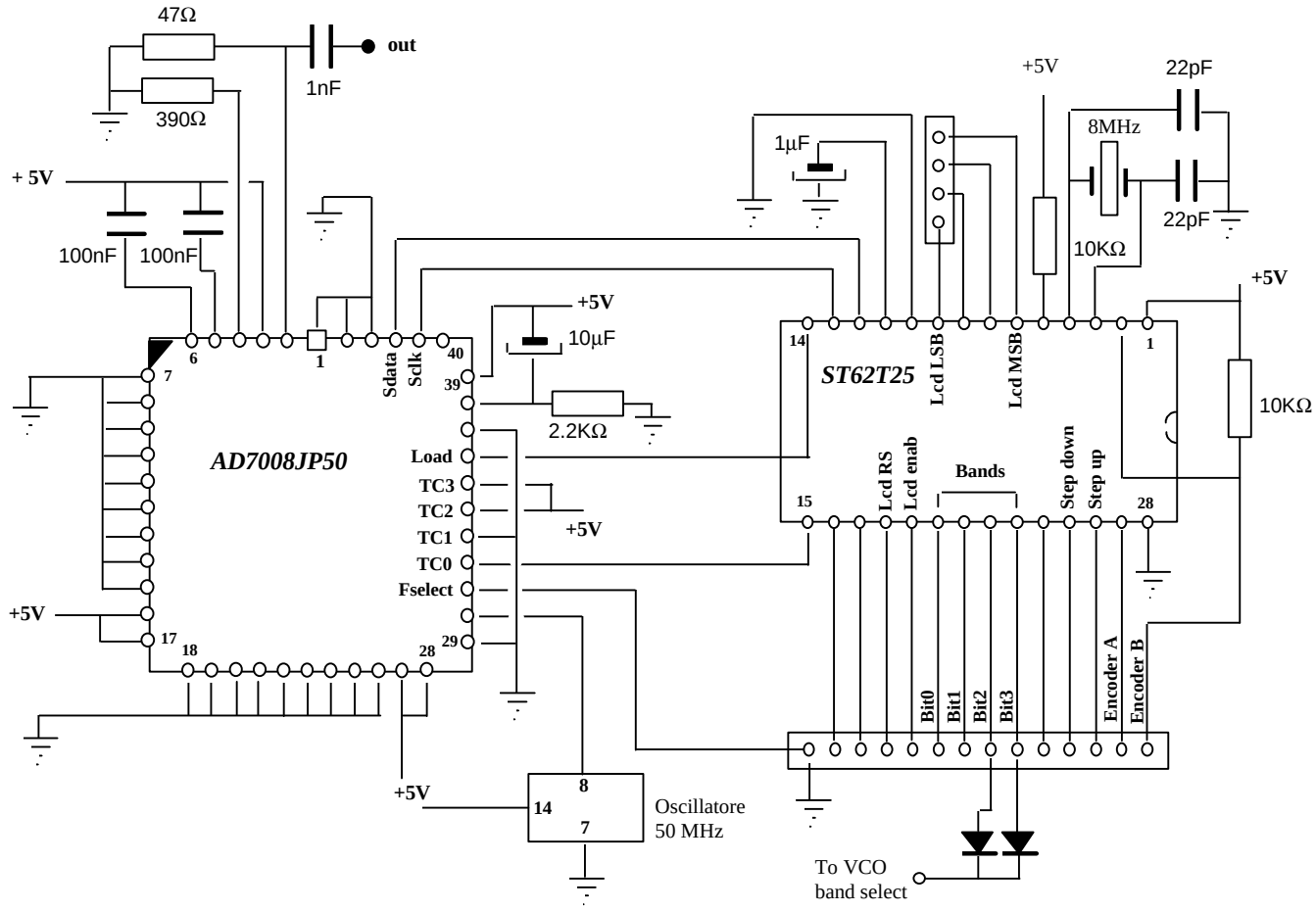
This module is composed by two oscillators, the switching circuit and the output buffers.
Because of the wide frequency range (from 10.8 to 39 Mhz) it was necessary to employ two separate oscillators using high capacity varicap diodes (BB112, MVAM115). The digital output (band) from the DDS module can be used to switch the two oscillators (as explained below).
Two high level outputs are provided (about 3 V pp) to drive the PLL divider and the RX mixer (mosfet), one low level output (about 300 mV) may be used to drive the TX mixer (MC1496).
L1 is composed by 16 turns of enameled copper wire, 0.5 mm diameter, wound on a 5 mm diameter plastic stand with ferrite core.
L2 is composed by 9 turns of the same wire
To tune this unit, I suggest to drive the two control inputs (marked *from PLL*) with a variable voltage ranging from 1 to 10 volts. So doing you should obtain the full frequency coverage (from 10 to 22 Mhz with L1, from 20 to 40 Mhz with L2) at an almost constant ouput level. Remember to use a shielded cable (RG174) for the connections to the PLL module both for the RF signal and for the control voltage.

The PLL Module



This module is composed by the x 64 HCMOS divider (CMOS 4046), an LM358 operational amplifier working as a level translator for the VCO control voltage (from 5 to 10 V) and the loop filter. There is also a 7805 regulator wich may be fixed with a screw to the cabinet to sink the heat, after positioning the PCB (under the DDS module).
The loop is stable and the lock is fast, also owing to the high value of the frequency used as reference.
A special attention was paid to the stabilization of power supply, so avoiding any frequency modulation during the TX modulation peaks.
The module shouldn't require any tuning, verify only the voltage on pin 1 of the 74HC393 IC, it should be about 2 V with no input signal. The minimun input signal required is about 2 V pp. The lighting of a LED indicates the PLL LOCK condition.
This module, as I already saw, is stacked under the DDS module into the same little metal cabinet.

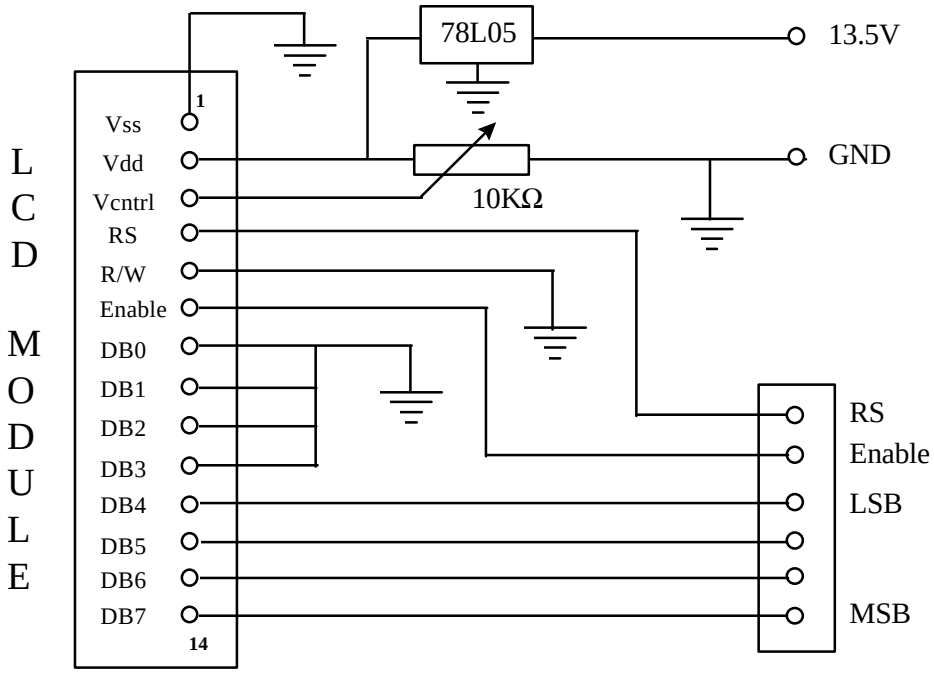
The DDS module



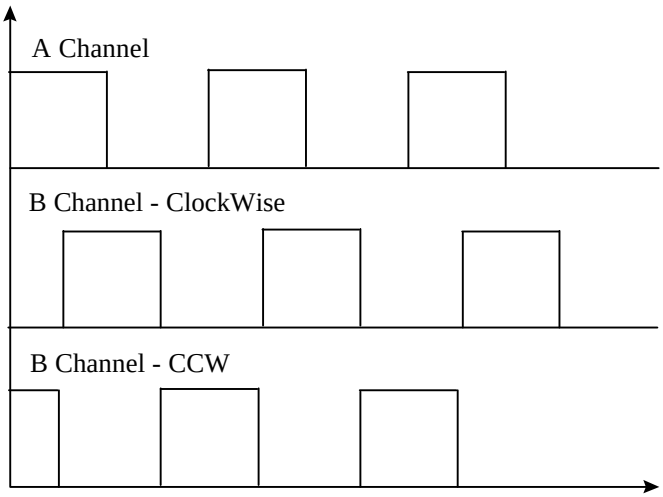
This module is composed by the DDS AD7008JP50 unit, the ST62T25 (or ST62E25) microprocessor and few other components. Be careful while soldering on the thin traces around the DDS socket. Two strip connectors and flat cables are employed to reach the external devices (LCD, encoder, ...).
The BANDS output is BCD coded and you'll have to decode it to drive an external switching circuitry, I employed a TL084 operational amplifier as a level translator and a CMOS 4028 BCD to DECIMAL decoder.
The VCO BAND SELECT pin may be driven connecting two diodes as shown in the schematic.
Pin 1 of the main connector (FSELECT) must be grounded (in a future software version it will be used to implement the SPLIT functions). Other not connected pins will be used to link an external memory device (ST93C66).

Additional Devices

The following schematic refers to a standard LCD display connections (14 pins), a 6 wire flat cable is used to connect the display to the DDS module.



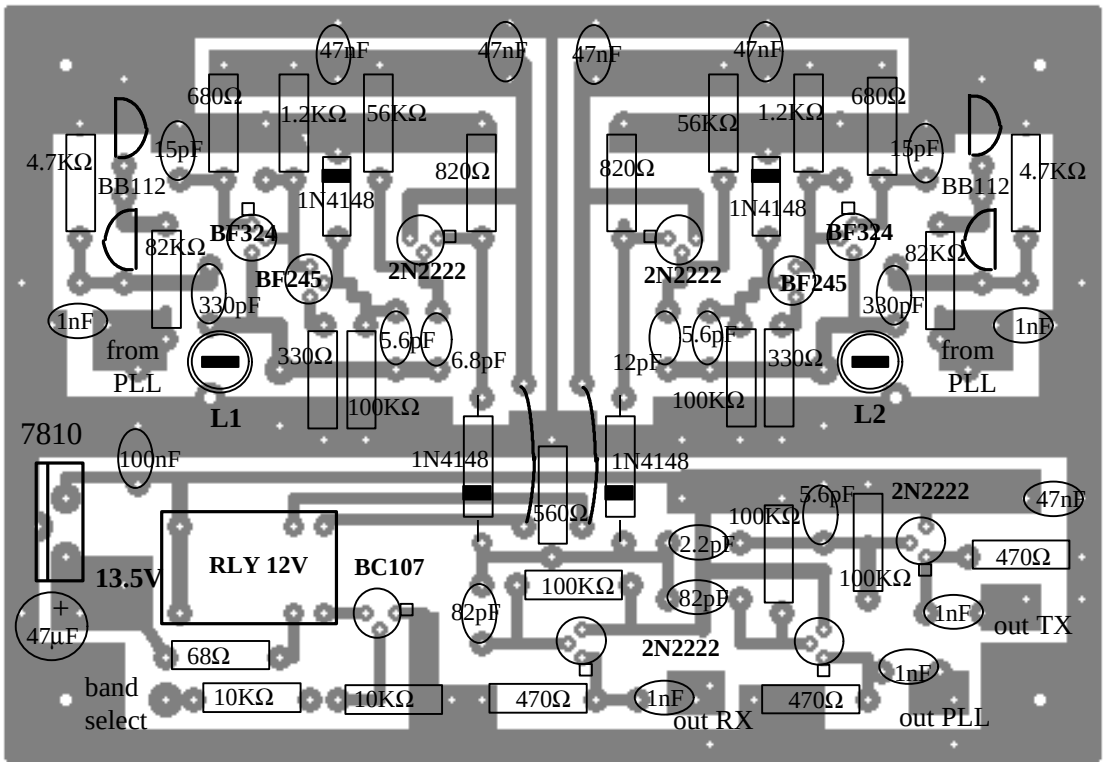
The optical encoder is a device equipped with two output channels (A and B) providing 90^0 phased (quadrature) square wawes. The phasing depends on the direction of rotation of the shaft, as shown in the following diagram.



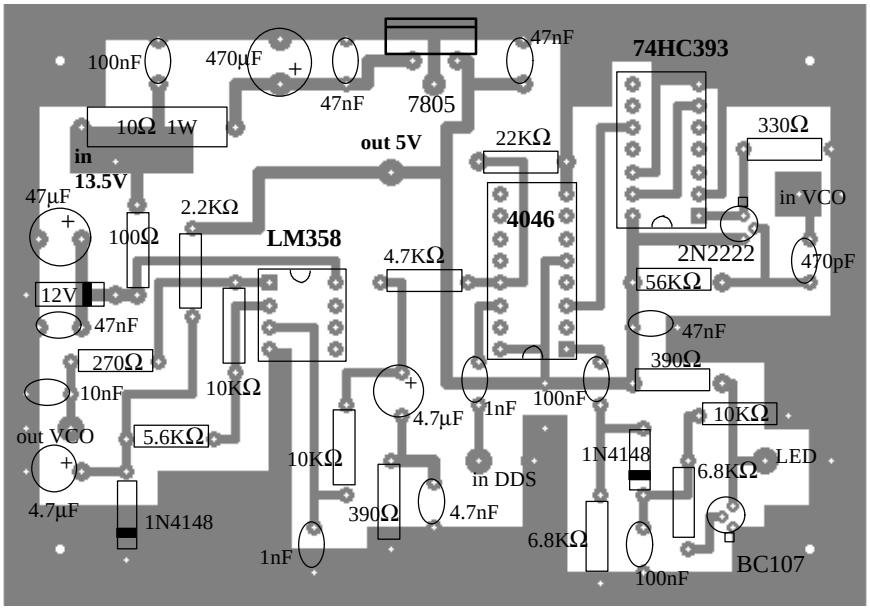
By sampling the B channel logic level while A channel's level is changing it is possible to know the rotation direction, while the number of pulses indicates the rotation amount. The connection to the DDS module is made with a 4 wires bus (ground, +5V and the two channels).

The assembly of the three modules

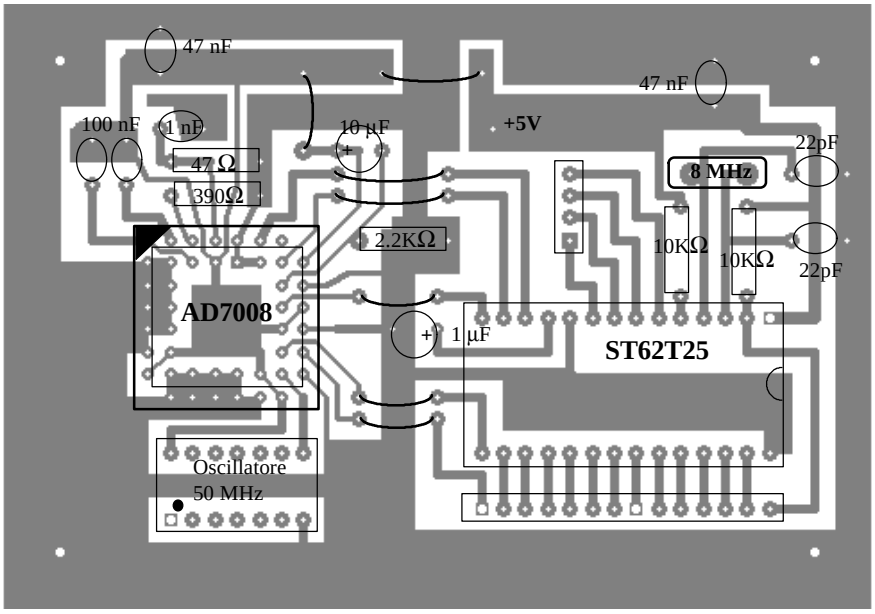
The VCO module (real dimension 97x67 mm)



The PLL module (real dimensions 97x67 mm)



The DDS module (real dimensions 97x67 mm)



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CIRCAD : http://www.holophase.com/
about LCD modules : http://www.eio.com/lcdintro.htm#data
Components info : http://www2.arnes.si/~uljfer3/elect/index.html

To get the CIRCAD PCB files, the ST62 software or other informations contact me at my E-mail address.