The 'Heaviside' Amplifier

Theory and Practice[1,2]

Riad S. Wahby

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Contents

[1]Thanks to Dylan Hester for his audiophile perspective and "confessional debugging," without which I might have overlooked several subtle practical issues.

[2]Oliver Heaviside is an extraordinarily interesting character, whose influences in mathematics, electrical engineering, and physics are largely underappreciated. A quick glance over his Wikipedia biography should prove a good starting point for further reading on this most extraordinary gentleman.

1 Introduction

The Heaviside is a high performance DC-coupled hybrid pre/headphone amplifier. It makes extensive use of operational amplifier design methodologies to achieve high open-loop gain and PSRR, stable biasing, flat frequency response, and low distortion. By employing a fixed inverting gain and highly optimized frequency compensation, good stability and wide bandwidth are achieved ($\phi_{\mathrm{m}} = 60°$ at 280 kHz). A novel topology employing solid-state cascodes with an offset-compensated vacuum tube differential pair achieves high gain in the input stage. This allows for a low gain, highly linear second stage and ensures that the input pair dominates the sonic characteristics of the amplifier.

2 Theory of operation

Figure 1 illustrates the topology of one Heaviside channel (the bias circuit is shared between channels). The 12AX7 triodes are biased at 1 mA each by the 2N3904 tail current source. The 300 Ω resistors and 5 kΩ potentiometer allow the input offset voltage to be trimmed, which minimizes offset and distortion arising from input stage mismatch. The ZTX458 cascode devices bias the 12AX7 plates to a very stable, ground-referred 220 V. Along with the regulated 295 V rail, this ensures excellent PSRR and very high (54 dB) gain in the first stage, while allowing ample headroom for the heavily degenerated current mirror load.

The second stage uses a telescopic emitter-coupled pair with substantial degeneration, which provides both a level shifter and 1 mA bias for the 2N3904-based V_{be} multiplier. This "floating battery" ensures about one diode drop across the 44 Ω emitter resistance, resulting in approximately 15 mA through the output transistors at all times. The 2N3904 and 2N3906 transistors across the emitter resistors provide output over-current protection by stealing base current from the output transistors when the output current grows too large. The current limit is set by the 4.99 Ω resistors, which limit current to $\frac{600\ \mathrm{mV}}{4.99\ \Omega} \approx 120$ mA.

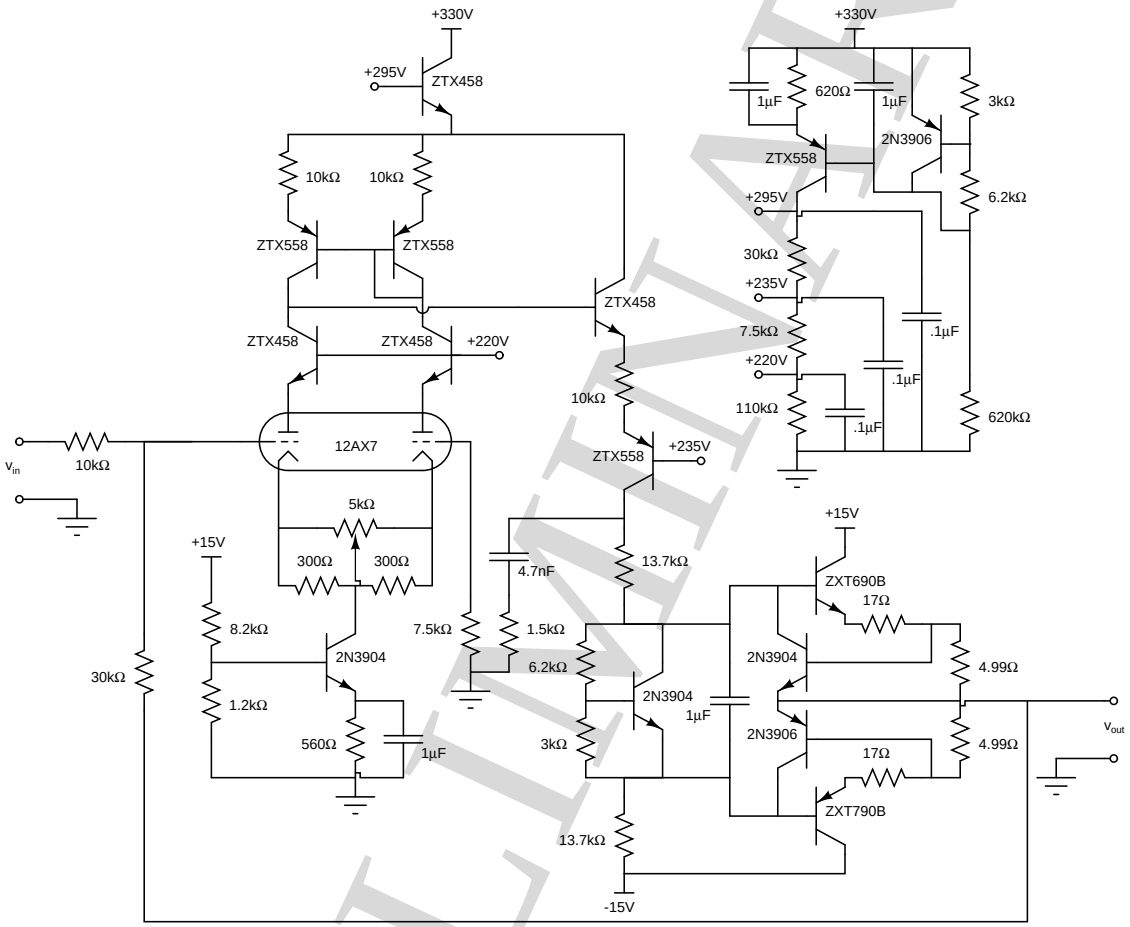

Figure 1: One channel of the Heaviside amplifier.

3 Simulation results

This design was optimized using the HSPICE circuit simulator. Unfortunately, HSPICE has no native vacuum tube modelling capability, so a behavioral subcircuit model was first developed after the work done by Norman Koren[3]. Using this model, small signal and transient analyses were performed to optimize the frequency compensation and distortion characteristics of the amplifier.

3.1 12AX7 HSPICE model

To model the 12AX7, the following subcircuit was used:

```
.subckt t12ax7 p g k

.param mu=100
.param ex=1.4
.param kg1=1060
.param kp=600
.param kvb=300

e101 101 0 value='kp * ( (1/mu) + (v(g,k) / sqrt( kvb + pwr( abs( v(p,k) ),2 ) )) )'
e102 102 0 value='1 + exp(v(101,0))'
e103 103 0 value='(v(p,k)/kp) * log(v(102,0))'
E104 104 0 value='1e-6*pwr( min( (v(g,k) + abs(v(g,k)))/2 + 2 , 9999 ), 1.5 )'
Gp   p   k value='v(103,0)* (ex/kg1) * (1 + sgn(v(103,0)))'
Gg   g   k value='v(104,0)'
Cgk  g   k 2.3p
Cgp  g   p 2.4p
Cpk  p   k .9p

.ends t12ax7
```

3.2 AC analysis

AC analysis was performed using the above tube model, along with transistor models from Zetex and Fairchild. To achieve a high open loop crossover frequency, a pole and zero are

[3]See http://www.normankoren.com/Audio/Tubemodspice_article.html

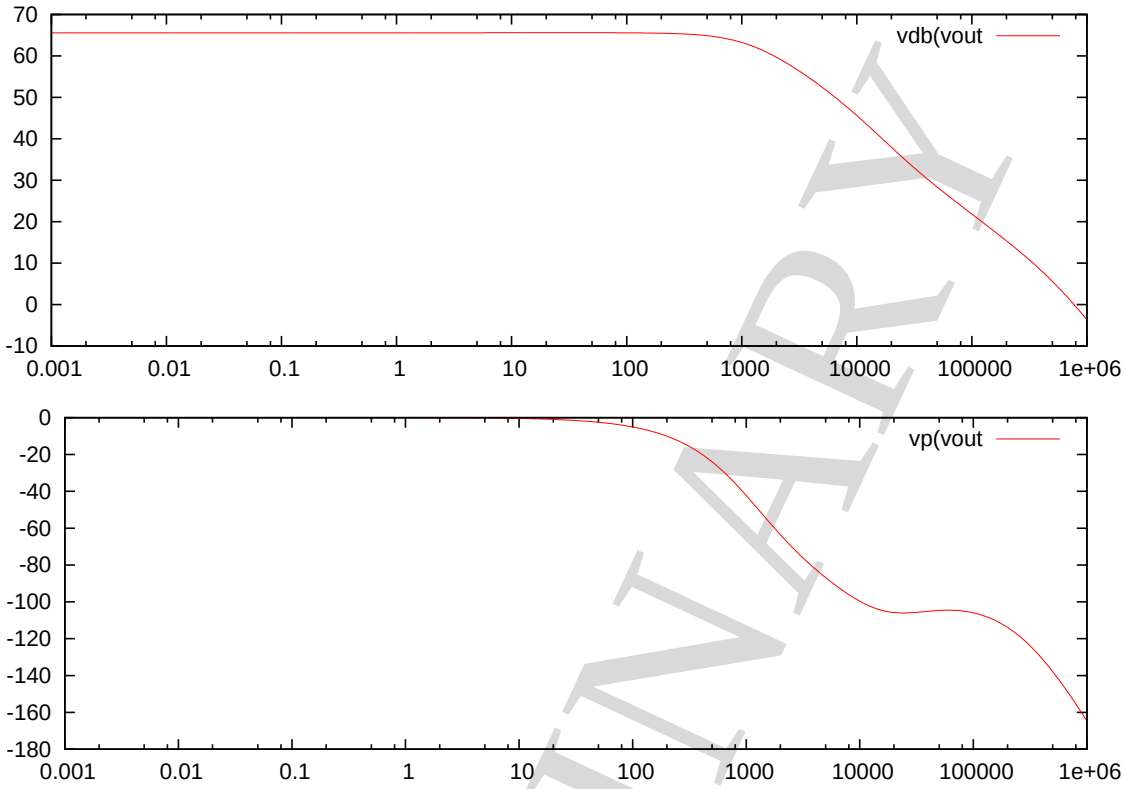

Figure 2: Open loop frequency response.

added via the series 4.7 nF capacitor and 1.5 kΩ resistor. Along with the dominant pole in the uncompensated circuit, the compensated open loop frequency response is as depicted in Fig. 2. Since this amplifier is designed for operation with an inverting gain of 3, the stability of the amplifier in closed loop is determined by the phase shift at 12 dB. From the figure, this results in about 60 degrees of phase margin at 280 kHz. See section 5 for the full SPICE deck.

3.3 Transient analysis

Transient simulations to verify distortion performance were also performed. With 2 V RMS input at 1 kHz, total harmonic distortion is less than .0013%:

```
fourier components of transient response v(vout)
dc component =  -1.247E-04
harmonic   frequency  fourier    normalized  phase     normalized
   no         (hz)    component  component   (deg)     phase (deg)


     1      9.999e+02  8.467e+00  1.000e+00  1.798e+02    0.
     2      2.000e+03  5.021e-05  5.930e-06 -1.540e+02 -3.339e+02
     3      3.000e+03  6.910e-05  8.160e-06 -3.901e+01 -2.189e+02
     4      4.000e+03  3.558e-05  4.202e-06 -7.788e+01 -2.577e+02
     5      5.000e+03  6.200e-06  7.322e-07 -8.446e+01 -2.643e+02
     6      6.000e+03  4.359e-05  5.148e-06 -1.073e+02 -2.872e+02
     7      7.000e+03  1.531e-05  1.808e-06  9.154e+01 -8.834e+01
     8      8.000e+03  2.653e-05  3.134e-06 -6.875e+01 -2.486e+02
     9      9.000e+03  7.100e-06  8.385e-07  6.851e+01 -1.113e+02


    total harmonic distortion =   1.266e-03  percent
```

The distortion contains substantial even order components, indicating that as expected, the tube differential pair dominates the distortion profile.

4 Implementation and Laboratory Results

4.1 Ancillary Circuits

4.1.1 Power Supply

The power supply produces an unregulated high voltage rail of approximately 330 V, plus a regulated ±15 V to supply the preamplifier op-amps, offset detector, and tube filaments. In addition, the regulated low voltage rails are filtered with an LC section to produce a supply which drives the output stage while keeping audio ripple current from flowing across the PCB.

The bias generator stage in Fig. 1 produces a regulated ground-referenced 295 V high voltage rail. The only circuits driven directly from the unregulated 330 V rail are the bias generator and the emitter followers which buffer the ground-referenced 295 V.

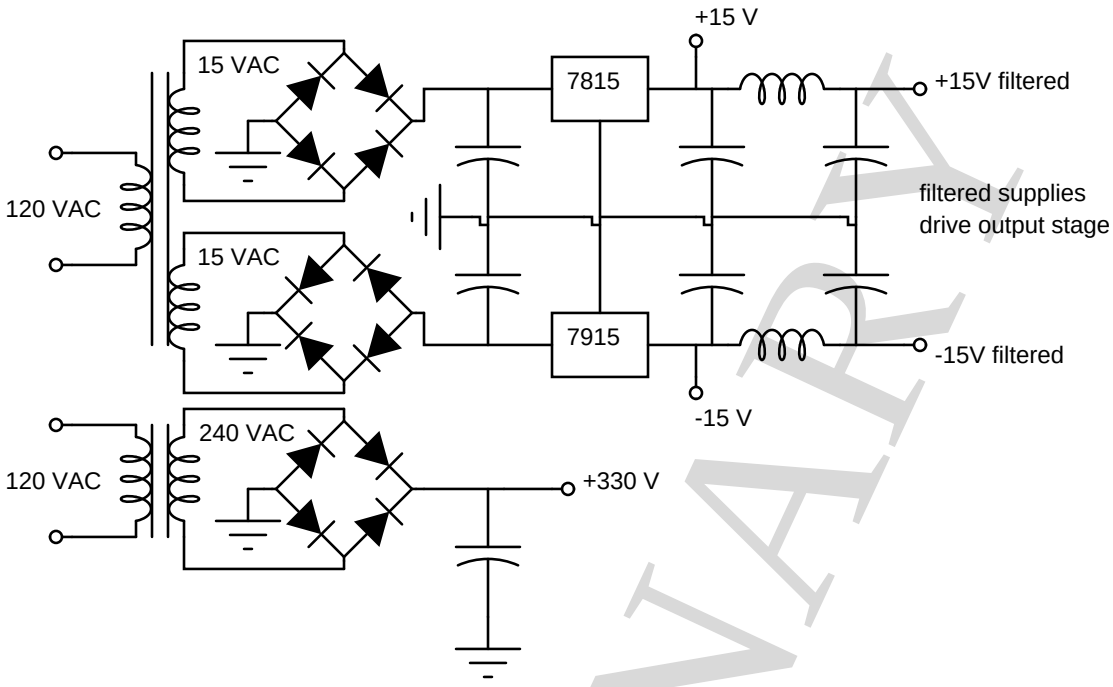

Figure 3: Power supply for the Heaviside amplifier.

4.1.2 Volume Control

A significant advantage of running the Heaviside amplifier in the inverting configuration is that the input common mode voltage remains constant, making the first stage substantially more linear. Unfortunately, it also means that the input impedance to the amplifier is only about as large as the input resistor; moreover, implementing volume control in this configuration will necessarily affect loop stability.

To achieve a constant, relatively high input impedance and provide volume control, an op-amp is used as a non-inverting buffer before the Heaviside stage. The op-amp is connected in a gain of two configuration so that op-amps that are not unity gain stable (e.g., the AD797) can be used. Moreover, on the PCB, footprints for both two single op-amps and one dual op-amp are provided; by populating one or the other, plus the accompanying feedback network, any SOIC op-amp with the standard pinout can be used. The implementation as tested herein uses the AD823 op-amp.

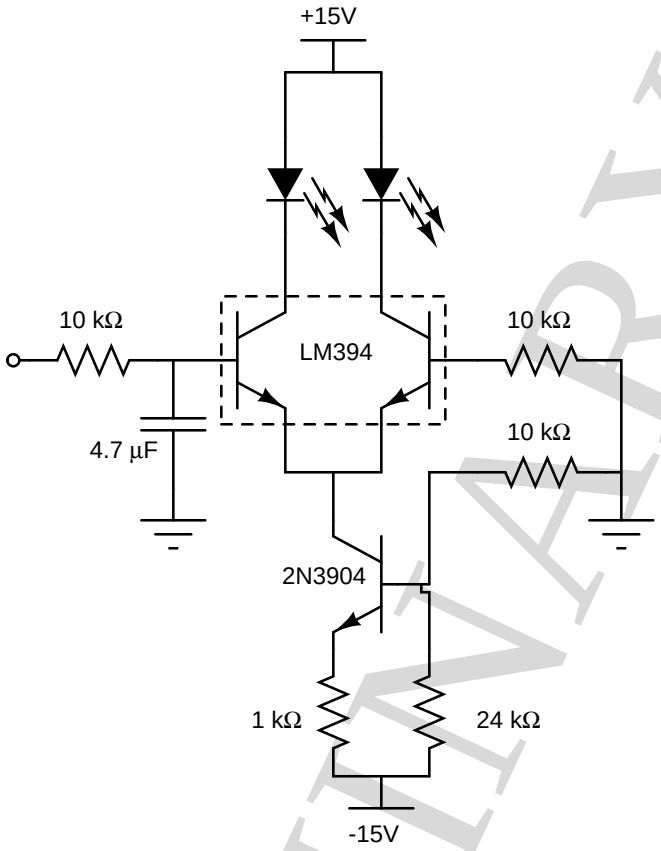

Figure 4: An offset indicator for trimming without a multimeter.

4.1.3 Offset Indicator

The Heaviside has no closed-loop offset control. This is intentional, since any such system would necessarily involve a rolloff in low frequency response and possible degradation of low-frequency linearity. The offset of the amplifier is relatively stable over temperature, but for additional peace of mind, an offset indicator circuit can be used to monitor the DC output voltage. Figure 4 shows the circuit as implemented; when the brightness of the two LEDs matches, the offset is minimal. With practice, this circuit can be used to trim the output offset to a few millivolts without the use of a multimeter.

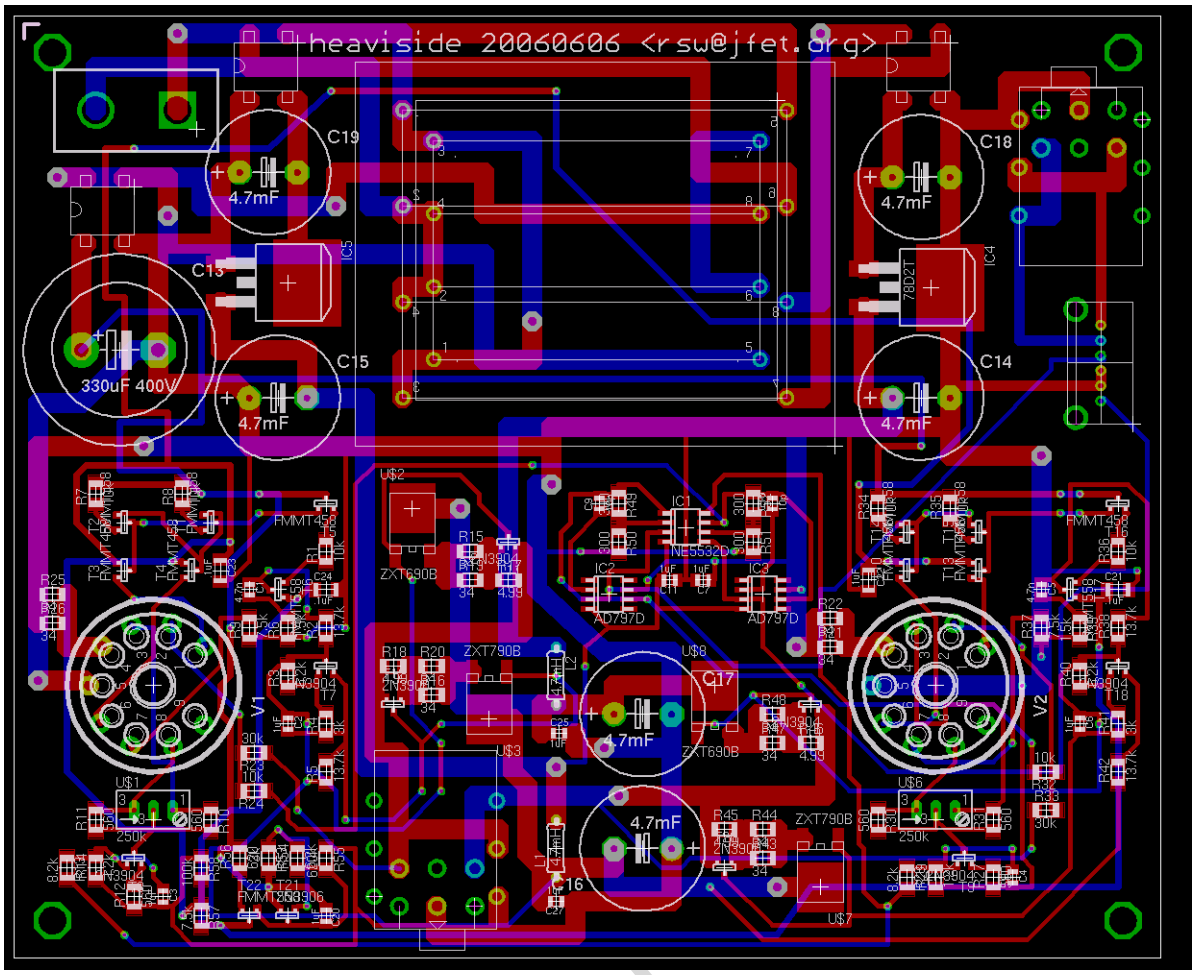

Figure 5: The Heaviside amplifier layout, revision 20060606.

This circuit is not included on the present version of the PCB layout; instead, it was built on perfboard and directly wired to the proper points on the circuit board. Future versions will incorporate it onboard.

4.2 PCB

Figure 5 depicts the layout of the Heaviside amplifier. This revision does not include the regulated 295 V rail; the change was made by modifying the PCB. Future revisions of the

board will include this modification. Surface mount components were used where possible to save space and hasten assembly.

The only unexpected consideration in this implementation was shielding the transformers. Since this board uses relatively cheap transformers instead of better shielded EIs or toroids, they leak a substantial amount of flux, inducing audible 60 Hz noise on the output. To combat this, the transformers were shielded with four layers (likely far more than necessary) of Advance Magnetics AD-MU-80 4 mil foil.

4.3 Laboratory Results

Once built, measurements were taken using an Audio Precision SYS-2722.

Dynamic range was determined by characterizing idle channel noise in the audio band, 20 Hz to 22 kHz. In this range, RMS noise voltage into a high impedance load was 56 μV. Full scale output voltage, given the $\pm$15 V rails on the output stage, is conservatively 7 V RMS. This gives $\frac{7}{56\times10^{-6}} = 102$ dB dynamic range. Note that usable dynamic range into low impedance headphones is less than this, since the output swing cannot exceed that which would drive maximum power into the phones.

Figure 6 shows THD+N versus frequency. The THD measurement accuracy near 120 Hz is likely degraded by the presence of power supply ripple at this frequency; with better flux isolation and lower power supply ripple, this effect should largely disappear (the idle channel noise, as measured above, includes this frequency range, and thus it is not expected that the ripple present in this envisagement should present any perceptable degradation of sound quality). Note that at the top of the frequency range, the harmonic distortion increases precipitously. However, these harmonics are outside the range of hearing, and as such do not contribute audible distortion. [TODO: add spectral plot of THD+N measurement at 15 kHz to demonstrate that, as claimed, there are not significantly more harmonics in the audio band with high frequency inputs.] Tests of the Heaviside with a wide range of music

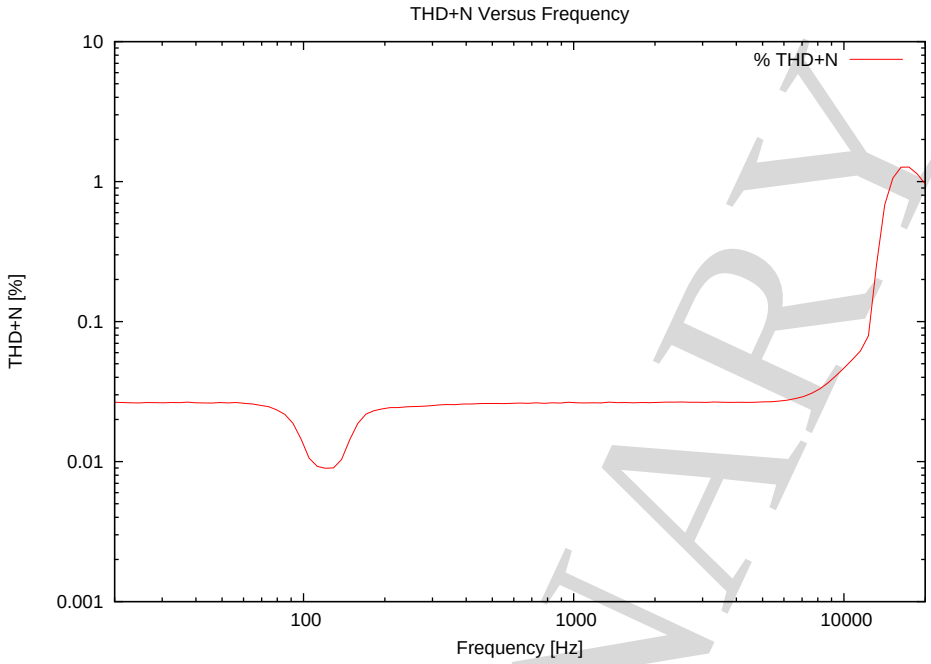

Figure 6: Heaviside amplifier THD+N as measured by the Audio Precision SYS-2722.

into two different headphones (Beyerdynamic DT-880 and Grado RS-2) bear out this claim: the top end sounds clear and undistorted.

Finally, the normalized frequency response of the amplifier is shown in Fig. 7. As expected, the -3 dB frequency is above 200 kHz. Frequency peaking is consistent with slightly less than 60 degrees of phase margin. This evidence is corroborated by the transient step response [TODO: add step response plot], which demonstrates 20 percent overshoot, also consistent with the expected phase margin.

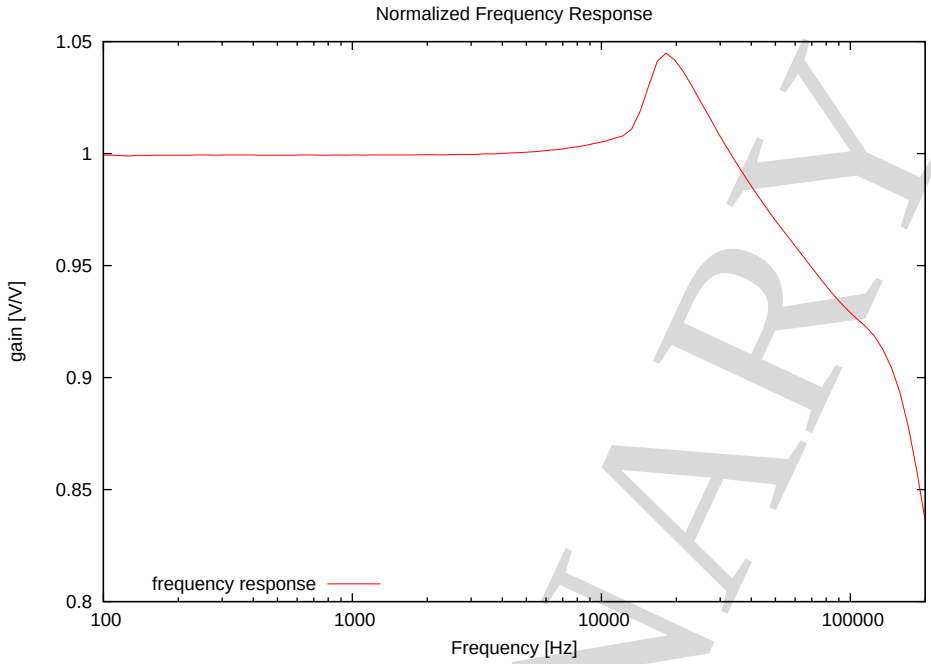

Figure 7: Heaviside amplifier frequency response as measured by the Audio Precision SYS-2722.

5 SPICE simulation deck

```
 headphone amp

 .options nomod post method=gear nopage ingold=2

.include '12ax7.inc'

.MODEL ztx790a PNP IS=1.09684E-12 NF=1.0102 BF=650 IKF=1.7 NK=0.75
+VAF=23.5 ISE=9.88593E-14 NE=1.47256 NR=1.00391 BR=270 IKR=0.2 VAR=30
+ISC=5.4933E-14 NC=1.07427 RB=0.055 RE=0.049 RC=0.078 CJC=96E-12
+MJC=0.495 VJC=0.67 CJE=275E-12 TF=0.75E-9 TR=10.8E-9 XTB=1.4
+TRE1=.0025 TRB1=.0025 TRC1=.0025

.MODEL ztx690b NPN IS =2.505E-12 NF =1.0058 BF =1360 IKF=1.3 VAF=35
+ISE=.24E-12 NE =1.38 NR =1.001 BR =125 IKR=1 VAR=8 ISC=.435E-12
+NC =1.213 RB =.2 RE =.043 RC =.04 CJC=54.3E-12 MJC=.475 VJC=.765
+CJE=247E-12 TF =.851E-9 TR =15.7E-9

.model ztx458 npn is=5.326791e-14 nf=0.992 bf=190 ikf=0.075
+vaf=1050 ise=2.1e-14 ne=1.385 nr=1.05 br=16.3 ikr=1.8 var=99
+isc=6.42e-12 nc=1.25 rb=0.5 re=0.224 rc=0.134 cjc=8.5e-12
+mjc=0.3966 vjc=0.4332 cje=122e-12 tf=1.66e-9 tr=8e-6
```

```
.model ztx558 pnp is=7.8443e-14 nf=0.99774 bf=200 ikf=0.096 vaf=349
+ise=3.35e-14 ne=1.689 nr=0.99784 br=3.4 ikr=0.15 var=82
+isc=9.42e-12 nc=1.05 rb=0.133 re=0.5725 rc=0.748 cjc=17.6e-12
+mjc=0.5932 vjc=0.9135 cje=110e-12 tf=1.13e-9 tr=75e-6

.model q2n3904  npn(is=6.734f xti=3 eg=1.11 vaf=74.03 bf=416.4 ne=1.259
+               ise=6.734f ikf=66.78m xtb=1.5 br=.7371 nc=2 isc=0 ikr=0 rc=1
+               cjc=3.638p mjc=.3085 vjc=.75 fc=.5 cje=4.493p mje=.2593 vje=.75
+               tr=239.5n tf=301.2p itf=.4 vtf=4 xtf=2 rb=10)

.model q2n3906  pnp(is=1.41f xti=3 eg=1.11 vaf=18.7 bf=180.7 ne=1.5 ise=0
+               ikf=80m xtb=1.5 br=4.977 nc=2 isc=0 ikr=0 rc=2.5 cjc=9.728p
+               mjc=.5776 vjc=.75 fc=.5 cje=8.063p mje=.3677 vje=.75 tr=33.42n
+               tf=179.3p itf=.4 vtf=4 xtf=6 rb=10)

* sources
vddh vddh 0 300
v15p vdd  0 15
v15m vss  0 -15
vin  vin  0 sin(0 '2*sqrt(2)' 1000 0 0) AC 1

.include hamp.ic0
*** cascode bias generator
rpbat1 vddh vpb 3e3
rpbat2 vpb vpc 6.2e3
qpbat vpc vpb vddh q2n3906
cpbat vpc 0 1e-6
rpbat vpc 0 620e3
qpi v240 vpc vpe ztx558
rpi vddh vpe 620
cpi vddh vpe 1e-6
c240 v240 0 .1e-6
r240 v240 v225 7.5e3
c225 v225 0 .1e-6
r225 v225 0 100e3

*** first stage
* tail current
rtailb1 vdd vqtb 8.2e3
rtailb2 vqtb 0 1.2e3
qtail vkbias vqtb vqte q2n3904
rtail vqte 0 560
ctail vqte 0 1e-6
* balancing resistors
.param rrtl=492.39567
*.param rrtl=492.35247
rtl vkbias vkl 'rrtl'
rtr vkbias vkr '1000-rrtl'
* diff pair and cascodes
xtl vcascl vin vkl t12ax7
xtr vcascr 0 vkr t12ax7
*xtl vcascl vinp vkl t12ax7
*xtr vcascr vinm vkr t12ax7
```

```
qcascl vop v225 vcascl ztx458
qcascr vom v225 vcascr ztx458
* top mirror
qmirl vop vop vmirl ztx558
qmirr vom vop vmirr ztx558
rmirl vmirl vddh 10e3
rmirr vmirr vddh 10e3

*** output stage
* emitter-coupled pair level shifter
qecpn vddh vom vomf ztx458
recp vomf vecppe 10e3
*cecp vomf vecppe .1e-9
qecpp vecppc v240 vecppe ztx558
ccomp vecppc vecppcr 4.7e-9
rcomp vecppcr 0 1.5e3
* floating battery bias
rbiast vecppc vfbatp 13.7e3
rbat1 vfbatp vfbatb 6.2e3
rbat2 vfbatb vfbatm 3e3
cfbat vfbatp vfbatm 1e-6
qbat vfbatp vfbatb vfbatm q2n3904
rbiasb vfbatm vss 13.7e3
* output transistors
qoutn vdd vfbatp voutn1 ztx690b
*qoutn vdd vfbatp voutn1 q2n2219a
routn1 voutn1 voutn 17
routn voutn vout 4.99
qprotn vfbatp voutn vout q2n3904
qoutp vss vfbatm voutp1 ztx790a
*qoutp vss vfbatm voutp1 q2n2905a
routp1 voutp1 voutp 17
routp voutp vout 4.99
qprotp vfbatm voutp vout q2n3906

*** feedback network
*rin vin vinm 10e3
*rfb vout vinm 30e3
*rp  vinp 0 7.5e3

rload vout 0 250

.op
*.tran 1u 5e-3
*.four 1e3 v(vout)
.ac dec 100 1e-3 1e6
.probe vdb(vout)
.probe vp(vout)

.end
```